Claims

What is claimed is:

1. An information handling system comprising:

a first node for:

detecting a first memory in the first node;

detecting a second memory in a second node coupled to the first node;

ensuring that a first set of contiguous addresses is mapped to a portion of the first memory, the first set of contiguous addresses each having a value lower than a four gigabyte address; and

ensuring a second set of contiguous addresses is mapped to a portion of the second memory, the second set of contiguous addresses each having a value lower than the four gigabyte address.

2. The information handling system of claim 1, wherein the first node is for:

reserving a third set of contiguous addresses that each have a value lower than the four gigabyte address.

3. The information handling system of claim 2, wherein the first node is for:

detecting a third memory in a third node coupled to the first node subsequent to the first node and the second node being booted; and

mapping the third set of contiguous addresses to a portion of the third memory.

4. The information handling system of claim 1, wherein the first node is for:

detecting a size of the first memory in the first node; and

determining a size of the portion of the first memory in response to the size of the first memory.

5. The information handling system of claim 4, wherein the first node is for:

detecting a size of the second memory in the second node; and

determining the size of the portion of the first memory and a size of the portion of the second memory in response to the size of the first memory and the size of the second memory.

6. The information handling system of claim 1, wherein the first node is for:

detecting a number of nodes that are coupled to the first node; and

determining a size of the portion of the first memory in response to the number of nodes.

7. The information handling system of claim 1, wherein the first node is for:

detecting a maximum number of nodes that may be coupled to the first node; and

determining a size of the portion of the first memory in response to the maximum number of nodes.

8. A method comprising:

detecting a first memory in a first node;

detecting a second memory in a second node coupled to the first node;

ensuring that a first set of contiguous addresses is mapped to a portion of the first memory, the first set of contiguous addresses each having a value lower than a four gigabyte address; and

ensuring a second set of contiguous addresses is mapped to a

portion of the second memory, the second set of contiguous addresses each having a value lower than the four gigabyte address.

9. The method of claim 8, further comprising:

reserving a third set of contiguous addresses that each have a value lower than the four gigabyte address.

10. The method of claim 9, further comprising:

detecting a third memory in a third node coupled to the first node subsequent to the first node and the second node being booted; and

mapping the third set of contiguous addresses to a portion of the third memory.

11. The method of claim 8, further comprising:

detecting a size of the first memory in the first node; and

determining a size of the portion of the first memory in response to the size of the first memory.

12. The method of claim 11, further comprising:

detecting a size of the second memory in the second node; and

determining the size of the portion of the first memory and a size of the portion of the second memory in response to the size of the first memory and the size of the second memory.

13. The method of claim 8, further comprising:

detecting a number of nodes that are coupled to the first node; and

determining a size of the portion of the first memory in response to the number of nodes.

14. The method of claim 8, further comprising:

detecting a maximum number of nodes that may be coupled to the first node; and

determining a size of the portion of the first memory in response to the maximum number of nodes.

15. A computer program product comprising:

a computer program processable by a first node to:

detect a first memory in the first node;

detect a second memory in a second node coupled to the first node;

ensure that a first set of contiguous addresses is mapped to a portion of the first memory, the first set of contiguous addresses each having a value lower than a four gigabyte address; and

ensure a second set of contiguous addresses is mapped to a portion of the second memory, the second set of contiguous addresses each having a value lower than the four gigabyte address; and

an apparatus from which the computer program is accessible by the first node.

16. The computer program product of claim 15, wherein the computer program is processable by the first node to:

reserve a third set of contiguous addresses that each have a value lower than the four gigabyte address.

17. The computer program product of claim 16, wherein the computer program is processable by the first node to:

detect a third memory in a third node coupled to the first node subsequent to the first node and the second node being booted; and

map the third set of contiguous addresses to a portion of the third memory.

18. The computer program product of claim 15, wherein the computer program is processable by the first node to:

detect a size of the first memory in the first node; and

determine a size of the portion of the first memory in response to the size of the first memory.

19. The computer program product of claim 18, wherein the computer program is processable by the first node to:

detect a size of the second memory in the second node; and

determine the size of the portion of the first memory and a size of the portion of the second memory in response to the size of the first memory and the size of the second memory.

20. The computer program product of claim 15, wherein the computer program is processable by the first node to:

detect a number of nodes that are coupled to the first node; and

determine a size of the portion of the first memory in response to the number of nodes.

21. The computer program product of claim 15, wherein the computer program is processable by the first node to:

detect a maximum number of nodes that may be coupled to the first node; and

determine a size of the portion of the first memory in response to the maximum number of nodes.

22. The computer program product of claim 15, wherein the computer program comprises a basic input output system (BIOS).